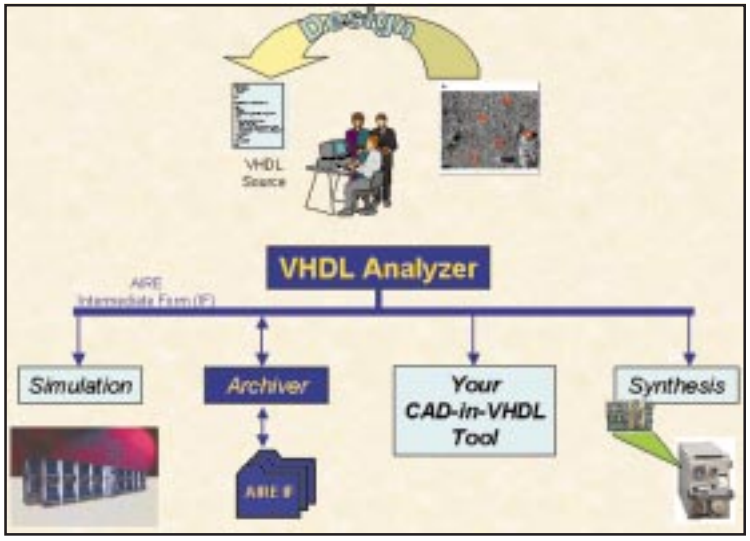
SAVANT Software Encourages Rapid Transition of New CAD Tools



Payoff

The Standard Analyzer of VHDL Applications for Next-Generation Technology (SAVANT) program reduces the government's research costs, freeing up more dollars for actual electronic design and tool research. The availability of an analyzer and library subsystem will dramatically promote additional research and development in computer-aided design (CAD) and its integration with VHSIC Hardware Description Language (VHDL). The software tools are free to universities and researchers, and can be licensed for inclusion in commercial products.

Accomplishment

An Information Directorate supported Small Business Innovative Research (SBIR) funded project with MTL Systems and the University of Cincinnati resulted in the development of freely available VHDL software tools for electronic design analysis and simulation. This project leveraged a front-end VHDL analyzer to translate source code into a standard intermediate representation allowing researchers to focus on the productivity enhancing back-end tools. These tools will support development of new electronic design tools and allow CAD applications to be developed faster, less costly and more accurately.

Background

VHDL was developed in the 1980's to provide a mechanism for design and support of Department of Defense (DoD) information systems for Very High Speed Integrated Circuits (VHSICs). Once a design is captured, it may be analyzed, simulated, and synthesized into hardware. To research and develop CAD tools based on VHDL, an analyzer is needed to translate source code into an intermediate representation from which back-end tools can be developed. The VHDL analyzers currently available from commercial vendors have proprietary intermediate representations that are non-standard, subject to change, poorly documented, and inhibit research. In addition, these analyzers are expensive, costing approximately $30,000. Researchers and tool developers must commit up-front to a single CAD vendor that restricts the development and interoperability of CAD tools. In order to promote VHDL research and usage, the Information Directorate received SBIR funding for a project called SAVANT. This program enables design tool interoperability having an open, object-oriented approach with several advantages over the current process of developing a VHDL analyzer. The SAVANT program permits researchers to focus on tool development, thereby encouraging rapid transition of new CAD tools. It also expands the VHDL designer base in universities since tools and training will be readily available to students.